Secondment Report (Virtual)

Name: ESR2.2 – Raphael SEGABINAZZI FERREIRA
IRP title: Innovative real-time operating system for error management for single- and multi-core units

From: BTU, Cottbus, Germany
To: IHP, Frankfurt Oder, Germany
Period: January 15 – April 15, 2020

Activities during the secondment

- **Scope and objectives**
  - On the usage of the SEU monitor [1] and the ageing sensor [2] for lifetime extension using fine-grained reconfiguration controlled by an Operating System (OS) enabled by the platform in [3].
  - Assisting the RESCUE Chip activities from the software/operating system perspective.
- **Activities**
  - Getting familiar with the SEU sensor [1] and the ageing sensor [2].
  - Brainstorm with Dr. Simevski and the ESR 1.2 (Junchao Chen) collecting ideas on how to assemble the sensors from [1] and [2] in the platform proposed in [3], as well as how to test and evaluate the platform.
  - Getting familiar with the intended RISC-V cores [4].
  - Understand the PULP platform [5]: configuration of its design variations.
  - Setting up the environment for software compilation and design simulation.
  - Porting the FreeRTOS to the RISC-V environment in the PULP platform.
- **Main results achieved**
  - Compiler toolchain for the intended RISC-V version generated.
  - RISC-V environment (running RI5CY core [4]) based in the PULPino platform [5] up and running for design simulations.
  - RISC-V environment based in the PULP platform up and running for design simulations.
  - FreeRTOS partially ported from PULPino to the PULP platform.
- **Next Steps**
  - Complete the port of the FreeRTOS to the intended RISC-V platform.
- **Optional request for support or a technology/tool available at host:**
  - IHP libraries
  - Waterbear Framework Access

Self-evaluation

Overall score: 4
I consider this secondment successful, with regards to the research objectives achieved, skills developed, supervision quality, diversity of the resources. (Agree = 5 … Disagree = 1)

Optional comments: The secondment started with the objectives to attach hardware sensors developed from IHP to units within a design developed by the ESR, after proper evaluation this activity was put “on-hold” due to a change in the scope. Another wide scope was the RESCUE chip and its activities. Here the ESR was not directly involved in generating a hardware IP but to assist the team in generating proper software for the platform. Finally, the secondment was very harmed by the pandemic, thus, most of the tasks needed to be accomplished remotely. Though, IHP provided remote access to its infrastructure, servers and tools. This point was very helpful for the development of the ESR activates.

Date of the report approval by the supervisor: 18th March 2021.

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References

[1] J.-C. Chen, M. Andjelkovic, A. Simevski, Y.-Q. Li, P. Skoncej, M. Krstic, Design of SRAM-based Low-Cost SEU Monitor for Self-Adaptive Multiprocessing Systems, Euromicro Conference on Digital System Design (DSD 2019), Chalkidiki, August 28 - 30, 2019, Greece.

[2] A. Simevski, R. Kraemer, M. Krstic, “Low-complexity integrated circuit aging monitor”, 14th IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems, 2011.

[3] R. Segabinazzi Ferreira and J. Nolte, “Low latency reconfiguration mechanism for fine-grained processor internal functional units,” in LATS 2019 - 20th IEEE Latin American Test Symposium, 2019.

[4] P. D. Schiavone et al., “Slow and steady wins the race? A comparison of ultra-low-power RISC-V cores for Internet-of-Things applications,” in 2017 27th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS), 2017, pp. 1–8.

[5] PULP Platform, available in https://www.pulp-platform.org, visited on March 18, 2021.

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