Secondment Report (*Virtual*)

ESR No. and Name : ESR1.3 - Nevin George
IRP Title : HW/SW fault tolerance methods driven by reliability and timing constraints

Host Institution : BTU, Cottbus, Germany
Visiting Institution : IHP, Frankfurt Oder, Germany
Intended Period : 15 January 2020 – 15 June 2020

Activities during the secondment

- **Scope and objectives:**
  - Creation of Chip based testbed for fault monitors in tandem with ESR 1.2 Junchao Chen (IHP, "Adaptive methods for fault tolerant embedded systems")
  - Generation of Fault Monitor Data for reliability assessment.
  - Application of Reliability assessment models (This scope must be limited, for practical reasons)
- **Activities:**
  - Assisting in setting up implementation and testbed for Verilator based simple system example implementations of RISC-V Ibex cores and further testbed creation/ modification[6];
  - Virtual RESCUE Chip tapeout plans agreed
  - Integration into RESCUE Chip (RISCV – with Ibex core) testbed if already available; else effort must be spent of testbed (simulation) creation also.
  - Familiarisation with monitor/sensor RTL implementations (Aging, Variation and SEU)[1][2][3][4][5].
- **Main Results Achieved:**
  - Implementation of RISC-V(Ibex) core based Evaluation Testbench, during RESCUE chip project participation; for baseline evaluation numbers
  - Virtual Chip tapeout plan established
- **Next Steps**
  - Updated versions of virtual tapeouts
  - Fault Injection platforms and assessment for fault monitors
- **Optional request for support or a technology/tool available at host:**
  - Waterbear Framework Access
  - IHP Libraries Access

Self-evaluation

Overall score: 4
I consider this secondment to be successful, with regards to the research objectives achieved, skills developed, supervision quality, diversity of the resources. (Agree = 5 … Disagree = 1)

Optional comments:
The secondment had a wide scope especially including the RESCUE chip project. A lot of the intended travel was also impeded due to the pandemic situation, but resolved with remote work. The adaption of fault monitor data from ESR 1.2 still is a work in progress.

Date of the report approval by the supervisor: - 12th March 2021

The RESCUE ETN project has received funding from the European Union's Horizon 2020 Programme under the Marie Skłodowska-Curie actions for research, technological development and demonstration, under grant n. 722325.

References:

[1] A. Simevski, R. Kraemer, and M. Krstic, “Low-complexity integrated circuit aging monitor,” in *14th IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems*, 2011, pp. 121–125.

[2] D. Ernst *et al.*, “Razor: circuit-level correction of timing errors for low-power operation,” *IEEE Micro*, vol. 24, no. 6, pp. 10–20, 2004.

[3] J. Chen, M. Andjelkovic, A. Simevski, Y. Li, P. Skoncej, and M. Krstic, “Design of SRAM-Based Low-Cost SEU Monitor for Self-Adaptive Multiprocessing Systems,” in *2019 22nd Euromicro Conference on Digital System Design (DSD)*, 2019, pp. 514–521.

[4] M. R. Choudhury, V. Chandra, R. C. Aitken, and K. Mohanram, “Time-borrowing circuit designs and hardware prototyping for timing error resilience,” *IEEE Trans. Comput.*, vol. 63, no. 2, pp. 497–509, 2014.

[5] S. Kim and M. Seok, “Variation-Tolerant, Ultra-Low-Voltage Microprocessor With a Low-Overhead, Within-a-Cycle In-Situ Timing-Error Detection and Correction Technique,” *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1478–1490, 2015.

[6] P. D. Schiavone *et al.*, “Slow and steady wins the race? A comparison of ultra-low-power RISC-V cores for Internet-of-Things applications,” in *2017 27th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, 2017, pp. 1–8.

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