Secondment report

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IRP title: Effective techniques for secure and reliable system validation
From: PDT
To: TUT
Period: 17th March – 14th April, 2019

Activities during the secondment

- **Scope and objectives.**

The Negative Bias Temperature Instability (NBTI) phenomenon is one of the main reliability issues in today's nanoelectronic systems. It causes increase in threshold voltage of pMOS transistors, thus degrading signal propagation delay in logic paths between flip-flops. Recently, IEEE published a new standard IEEE 1687 for Reconfigurable Scan Networks (RSN) to facilitate access to embedded instrumentation within an integrated circuit. In the field, the RSN infrastructure is often exploited for fault-management in failure-sensitive critical parts of the system. Therefore, the severity level of a fault in the RSN itself is very high, thus, amplifying the impact of the reliability issues caused by the aforementioned effect. Activities performed during this secondment were the first attempt to address above issues.

- **Activities.**

In collaboration with ESR 4.3, zamiaCad tool was used in order to perform gate-level simulation. As a result, signal toggling activity was recorded and used with the NBTI-model in [1] to evaluate aging effect on combinational logic present in RSNs. We developed a case study in order to examine the longest critical path and develop an algorithm for reducing the aging effect on it.

- **Main results achieved.**

Paper was written describing the analysis and the mitigation technique. Case study was presented, and experimental results given for some ITC'16 benchmarks. The paper was published and presented at the 27th IFIP/IEEE International Conference on Very Large Scale Integration, October 6-9, Peru

- **Next steps.**

Extending the analysis for examining the effect under different conditions (temperature and voltage) and comparing the aging effect with the rest of the circuit.

Self-evaluation

Overall score: 4
I consider this secondment successful, with regards to the research objectives achieved, skills developed, supervision quality, diversity of the resources. (Agree = 5 … Disagree = 1)
Optional comments: (text)

Date of the report approval by the supervisor: 18/11/2019

[1] M. Jenihhin et al., "Identification and rejuvenation of nbti-critical logic paths in nanoscale circuits," Journal of Electronic Testing, vol. 32, no. 3, pp. 273–289, Jun 2016

The RESCUE ETN project has received funding from the European Union's Horizon 2020 Programme under the Marie Skłodowska-Curie actions for research, technological development and demonstration, under grant n. 722325.