Name: ESR4.2 Ahmet Cagri Bagbaba
IRP title: **EDA Tools and methodologies for high quality nanoelectronics systems**
From: CDNS
To: PDT
Period: 29. April - 17. May, 2019

Activities during the secondment

▪ **Scope and objectives:**
Discussions about AutoSoC, multi-point fault injection, and collaboration with ESR1.4 Josie Esteban Rodriguez Condia (PDT).

▪ **Activities:**
ESR4.2 gave a demo presentation about Cadence functional safety tool environment. Then, possible future research topics on AutoSoC and multi-point fault injection was discussed with Prof. Matteo Sonza Reorda. Also, the first experiments were started and discussed.

▪ **Main results achieved:**
Working environment and setup was done to work on multi-point fault injection and GPGPU. Some modules of GPGPU were synthesized and first gate-level rt-level logic simulations were done in order to be sure that functionality is still correct. Then, first fault injection campaigns were completed on the synthesized modules of GPGPU.

▪ **Next steps:**
   o Multi-point fault injection: Fault masking on sequential circuits will be analysed. Additionally, effect of double faults will be analysed on safety related CPUs.
   o GPGPU: Fault injection effects on each instruction will be investigated on RTL and gate-level to understand what the correlation is between different abstraction levels. Some other modules of GPGPU will be synthesized and investigated.

▪ **Optional request for support or a technology/tool available at host:** No

Self-evaluation
Overall score: 5
Optional comments: None

Date of the report approval by the supervisor: 19.11.2019