Secondment report

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IRP title: **Open-source EDA tools for design quality and reliability automation using zamiaCAD**
From: TUT
To: TUD
Period: February 09 – March 16, 2019

Activities during the secondment

- **Scope and objectives:**
  - Define the experimental setup that is be able to run realistic programs and record cycle accurate memory access patterns (read/write)
  - Prepare a set of memory access patterns
- **Activities:**
  - Deciding on CPU instruction set architecture, simulation level, CPU implementation
  - Trying several implementations considering popularity, simulation setup and C compiler setup
  - Finding realistic benchmarks (programs) in C
  - Testing and modifying benchmarks to run on our experiment setup
  - Implementing a memory tracer module to record memory activity
- **Main results achieved:**
  - We decided to use RISC-V instruction set architecture and RI5CY CPU core together with Pulpino microcontroller project
  - Tested benchmarks from MiBench, and modified them to run with the experiment setup
  - Implemented a memory tracer module
  - Generated first set of memory access patterns
- **Next steps:**
  - Test generated memory access patterns with zamiaCAD to estimate rejuvenation potential
  - Add a periodic interrupt routine to benchmarks to run a rejuvenation workload
  - Add more benchmarks to demonstrate wider range of outcomes in the results

- **Optional request for support or a technology/tool available at host:** No.

Self-evaluation

Overall score: 5
I consider this secondment successful, with regards to the research objectives achieved, skills developed, supervision quality, diversity of the resources. (Agree = 5 … Disagree = 1)
Optional comments:

Date of the report approval by the supervisor: 10.02.2020

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