RESCUE
European Training Network

INTERDEPENDENT CHALLENGES OF RELIABILITY, SECURITY AND QUALITY IN NANOELECTRONIC SYSTEMS DESIGN

2017–2021

PhD student researcher positions
(Early-Stage Researchers)

www.rescue-etn.eu

H2020–MSCA–ITN–2016 / MSCA–ITN–ETN

HORIZON 2020 MARIE CURIE ACTIONS

The RESCUE ETN project has received funding from the European Union's Horizon 2020 Programme under the Marie Curie-Skłodowska actions for research, technological development and demonstration, under grant n. 722325.

About the project

RESCUE action advances scientific competences and establishes an innovative training for **Interdependent Challenges of Reliability, Security and Quality in Nanoelectronic Systems Design.**

Today, nanoelectronic systems are at the core of all industry sectors and deployed in life-critical application domains, such as healthcare, transportation, automotive and security, serving societal needs in Europe. They are being combined into Internet-of-Things (IoT) and Cyber-Physical Systems and, ultimately, represent the physical backbone of our increasingly digitised world. Here, the impact and consequences of in-field failures, security attacks or hardware defects can be catastrophic. At the same time, they are getting very hard to avoid due to the trends of extreme complexity and miniaturisation at the doorstep of physical limits.

The novel training-through-research platform will rescue and enhance design of complex systems at the next generation nanoelectronics technologies by addressing the demanding and mutually dependent aspects of **reliability**, **security** and **quality**, as well as corresponding **electronic design automation tools**. It will to provide recruited Early-Stage Researchers (ESRs) with innovative training in the involved disciplines and beyond, such that they will not only be able to face today and future challenges in nanoelectronics design but also be innovative, creative, and more importantly - have an entrepreneurial mentality. The consortium consists of leading European research groups competent to tackle the interdependent challenges in a holistic manner and to train **new top-notch interdisciplinary professionals**. The ITN is excellently balanced in terms of state-of-the-art academic and industrial training and research facilities.

Project duration: **April 1, 2017 – March 31, 2021 (4 years)**

Total budget: **3.76 MEUR**

ESR recruitment period: **36 months**

Application process: **during April 1 – June 10, 2017 (early application leaves more time for communication)**

All the ESRs are planned to start in September/October 2017.

Eligibility

Requirement 1 (early-stage researchers): Applicants must, at the date of recruitment by RESCUE, be in the first four years (full-time equivalent research experience measured from the date when the researcher obtained the degree entitling him/her to embark on a doctorate) of their research careers and have not been awarded a doctoral degree.

Requirement 2 (mobility rule): Applicants must not have resided or carried out their main activity (work, studies, etc.) in the country of the recruiting institution for more than 12 months in the 3 years immediately before the recruitment date. This excludes short stays such as holidays or compulsory national service.

Requirement 3 (specialisation): Candidates should have a master level degree or equivalent in Computer Engineering, Computer Science, Electronics or related areas. Experience in the research scope of RESCUE is a vital asset.

Requirement 4 (English): Proficiency in English is essential, as it is the working language of the RESCUE network.

Conditions

- Full-time employment contracts at the selected RESCUE host institution for 36 month.
- The exact salary is to be confirmed upon appointment. The basic, gross amount is composed of Living Allowance = 3110 EUR/month (multiplied by the MSCA Country Correction Coefficients) AND Mobility/Family Allowance = 600 to 1100 EUR/month depending on the family situation.
- The recruited fellows are expected to complete their PhD theses by the end of their 3-year employment.

ESRs will actively participate in a 3-year RESCUE training program and deliver research results. The training includes

a) research training through individual research projects,
b) courses at the host institutions and events for scientific and transferable skills training,
c) training secondments to other RESCUE partners emphasizing cross-sectoral exposure.

ESRs will perform excellent in-depth research under cross-sectoral supervision the collaborative European Training Network.

Application procedure

Please see the details at the RESCUE website:
www.rescue-etn.eu

WP1 RELIABILITY

ESR 1.1 Test and Reliability of FinFET memories

Analysing both the aspect of quality and reliability of FinFET memories (e.g. at the 14nm technology node). Unique defects mechanism will be identified, including the Fin related, litho related, etc., as well as the impact of scaling, such as cell capacitance, intrinsic delays, etc. Fault models as well as appropriate test and design-for-testability schemes will be developed. In addition to that, quantification of reliability characteristics of the failure mechanisms and their impact on all parts of a memory system will be covered and appropriate mitigation schemes will be developed.

Recruitment host: Technical University of Delft, Delft, NL
Cross-sectoral co-supervision: IROC, FR
Contact: Prof. Dr. Said Hamdioui,
S.Hamdioui@tudelft.nl

ESR 1.2 Adaptive methods for fault-tolerant embedded systems

The ESR researcher will investigate adaptive methods for addressing fault tolerant properties of embedded systems. The focus will be on defining the methodology, which integrates the adaptive/dynamic use of fault tolerant methods at the different abstraction levels, including RTL, component and system level. The aim will be to enable dynamic trade-off between reliability, performance and power consumption, especially targeting the applications such as space/avionics and/or mixed-criticality systems implemented in the scaled technologies. The results (performance, achieved fault tolerance, reduced power consumption, increased lifetime) will be practically evaluated over test ASIC implementations and confirmed in measurements.

Recruitment host: IHP GmbH, Frankfurt (Oder), DE
Cross-sectoral co-supervision (PhD studies):
BTU Cottbus-Senftenberg, DE
Contact: Prof. Dr. Miloš Krstić,
krstic@ihp-microelectronics.com

ESR 1.3 HW/SW fault tolerance methods driven by reliability and timing constraints

The ESR project addresses reliability problems in nano-electronic circuits caused by both vulnerability to transient faults and by wear-out effects that may lead to early lifetime failures. The objectives will include fault tolerant design and lifetime extension by allocation of redundancy. Redundancy will be implemented using extra hardware or extra time, and optimised combinations of both. Since such concepts are costly in terms of hardware and power, the allocation of just the necessary level of fault tolerance, depending on signal importance and on timing reserves, will be investigated. Additionally, concepts of hierarchical system-level concepts of error resilience need to be supported.

Recruitment host: Computer Science, BTU Cottbus-Senftenberg, Cottbus, DE
Cross-sectoral co-supervision: IHP, DE
Contact: Prof. Dr. Heinrich T. Vierhaus, Heinrich.Vierhaus@b-tu.de

ESR 1.4 New Techniques for on-line fault detection

This ESR project will focus on the development and assessment of new techniques for detecting permanent faults arising during the operational phase of an electronic system, e.g., due to ageing phenomena. This task will be accomplished by resorting to suitable Design for Testability mechanisms, or to a functional approach, or to a clever combination of both. The activities of this ESR will build over the expertize in this area of the group of POLITO in cooperation with automotive and aerospace companies. Activities will explore new challenges which are recently becoming important, e.g., on-line test of GPU-based systems, compaction of functional test programs, identification of functionally untestable faults, generation of rejuvenation stimuli.

Recruitment host: Control and Computer Engineering, Politecnico di Torino, Turin, IT
Cross-sectoral co-supervision: Cadence, DE
Contact: Prof. Dr. Matteo SONZA REORDA, matteo.sonzareorda@polito.it

ESR 1.5 Reliable operation infrastructure for dynamic, high-dependability applications

This ESR project will consider high reliability applications for aerospace, automotive, HPC that need to work reliably and safely in aggressive working environments. The researcher will propose error management techniques, methodologies and instruments to detect and/or correct errors and reconfigure the design to meet the environmental constraints. The project will focus mostly on hardware capabilities that will be transparent to the application or assisted by a light software layer. This activity targets novel tools, methodologies and nanoelectronic system IPs for the management (detection and/or correction) of multiple categories of faults induced by the environment, the application or the design itself.

Recruitment host: IROC Technologies, Grenoble, FR
Cross-sectoral co-supervision (PhD studies): Politecnico di Torino, IT
Contact: Dr. Dan Alexandrescu,
dan.alexandrescu@iroctech.com

WP2 QUALITY

ESR 2.1 Effective techniques for secure and reliable systems validation

This ESR project will address validation of mechanisms to guarantee security and reliability of nanoelectronic systems. This task requires considering not only the space of all possible scenarios where the system is used, but also the possible hardware faults and external attacks the system is designed to face. Assessing the correct functionality of the system with such a huge combination of possibilities can only be done by combining different techniques coming from different communities (e.g., software validation, hardware validation, hardware testing) and exploiting different paradigms (e.g., simulation, formal techniques, evolutionary computation, design for validation). Test cases identified in cooperation with the industrial partners of RESCUE will be considered.

Recruitment host: Control and Computer Engineering, Politecnico di Torino, Turin, IT
Cross-sectoral co-supervision: IROC Technologies, FR
Contact: Prof. Dr. Matteo SONZA REORDA,
matteo.sonzareorda@polito.it

ESR 2.2 Innovative real-time operating system for error management for single- and multi-core units

Computer based systems of today mainly use several processor units already in local nodes. Typically, such units are available for customer electronics, implemented in very advanced nanotechnologies. The ESR will consider usage of such processors with high-reliability applications, as automotive electronics. The units will be configured to run with error detection and management and built-in redundancy for the elimination of permanent faults towards a long system lifetime. Error management concepts to be developed are based on unit that is able to monitor the overall status of the system and trigger actions of re-configuration and repair according to timing and workload.

Recruitment host: Computer Science, Brandenburgische TU Cottbus-Senftenberg, Cottbus, DE
Cross-sectoral co-supervision: IHP, DE
Contact: Prof. Dr. Heinrich T. Vierhaus
Heinrich.Vierhaus@b-tu.de

ESR 2.3 A synthetic, hierarchical abstraction approach for modelling and managing complex systems quality and reliability

The objective of the research is to significantly enhance and develop new statistical, probabilistic methods and algorithm for cell-level and circuit-level reliability analysis and management. In addition to the software, EDA-based fault and error evaluation in complex designs, the ESR will also use and improve hardware fault injection and failure analysis from field data. The researcher will contribute to an exhaustive EDA platform for the modelling and management of the reliability of complex design and systems. The proposed ESR aims at contributing towards the development of an industry-wide reliability framework and set of tools.

Recruitment host: IROC Technologies, Grenoble, FR
Cross-sectoral co-supervision (PhD studies): Tallinn UT, EE
Contact: Dr. Dan Alexandrescu,
dan.alexandrescu@iroctech.com

ESR 2.4 Functional and extra-functional verification and debug methods for complex nanoelectronic

The researcher will focus on design error functional verification and debug as well as verification of extra-functional interdependent aspects in complex nanoelectronic system design, such as security and reliability. The objectives include scalability, complexity and practical usability of the automated approaches for complex HW representations at RTL to ESL involving HW/SW interaction. The constraints posed by the design reliability and security aspects will be tackled using promising multi-view interference modelling and analysis approaches. The developed methodology is to be integrated into open-source frameworks, and possibly into industrial EDA tool flows by companies involved into the RESCUE network.

Recruitment host: Computer Systems, Tallinn University of Technology, Tallinn, EE
Cross-sectoral co-supervision: Cadence, DE
Contact: Dr. Maksim Jenihhin
maksim@ati.ttu.ee

WP3 SECURITY

ESR 3.1 A novel Physical Unclonable Functions technology

In this ESR project, fundamental research regarding future Physical Unclonable Function implementations will be performed. Detailed investigation will be done regarding the reproducibility, uniqueness and reliability of new PUFs. In combination with PUFs, security architecture design will be addressed. This project aims at realisation of the following targets:
1) Development of new PUF technology.
2) Evaluation of these new PUFs based on reliability, reproducibility and uniqueness.
3) Exploration of the new cryptographic primitives for creating a "root of trust" in hardware.

Recruitment host: Intrinsic-ID B.V., Eindhoven, NL
Cross-sectoral co-supervision (PhD studies): TU Delft, NL
Contact: Dr. Georgios Selimis,
georgios.selimis@intrinsic-id.com

ESR 3.2 Design approaches for tamper resistant crypto implementations

Side channel attacks are a very powerful means to extract keys from crypto devices, the subgroup of attacks to be investigated here are active attacks such as fault injection. The core idea is to research cryptographic algorithms implemented in different ways and to determine the sensitivity of this ASICs to fault attacks. First experiments shall be based on implementations using different variants of the operations and different types of gates. More alternatives are to be researched and all of them need to be evaluated. Based on the evaluation results implementation guidelines helping to prevent fault attacks shall be defined.

Recruitment host: IHP GmbH, Frankfurt (Oder), DE
Cross-sectoral co-supervision (PhD degree): BTU Cottbus-Senftenberg, DE
Contact: Prof. Dr. Miloš Krstić
krstic@ihp-microelectronics.com

ESR 3.3 Side-channel and Fault Attack resistant security primitives design

Physical unclonable function (PUF) technology is a leading one for unique authentication without having any secret/private key stored factually on the chip. On the other hand, side-channel and fault attacks are known for being used to hack hardware chips. Developing side-channel resistance solutions to make hacking of cryptographic primitives (such as PUFs and their required processing algorithms) is critical for a successful and sustainable deployment of PUF technology. The focus of the project will be on cryptographic primitives for PUF-based security systems able to resist these popular attacks and providing the highest level of security for the systems.

Recruitment host: Computer Engineering, Technical University of Delft, Delft, NL
Cross-sectoral co-supervision: Intrinsic-ID, NL
Contact: Prof. Dr. Said Hamdioui,
S.Hamdioui@tudelft.nl

WP4 EDA TOOLS AND METHODOLOGIES

ESR4.1 EDA tools and methodologies for reliable nanoelectronic systems

Traditional design and verification flows do not sufficiently consider physical effects of complex nanoelectronic MPSoCs over the extended lifetimes as they are found, e.g., in automotive domains. This results in overprovisioned or potentially unreliable systems. Looking at digital and mixed-signal systems at different abstraction-levels this research covers improved modeling and analysis techniques for catastrophic or degradation failures to capture their impact on design performance and functionality better. Developed concepts and methodologies are demonstrated as potentially automated proof-of-concepts within the Cadence Design & Functional Safety flow and the context of the ISO26262 using industrial case studies.

Recruitment host: Cadence Design Systems GmbH, Feldkirchen, DE
Cross-sectoral co-supervision (PhD studies): Tallinn UT, EE
Contact: Anton Klotz,
aklotz@cadence.com

ESR4.2 EDA tools and methodologies for high quality nanoelectronic systems

Functional safety becomes a first class citizen throughout the full design and verification process of complex systems and their embedded software. Architects and designers need fast ways to consistently consider dependability and fault tolerance across different abstraction levels and stages in the design flow. This research will consider meaningful system representations in simulation and emulation, enabling a quality-driven and potentially automated approach from analysis to addition of safety features and their efficient verification. Developed concepts and methodologies are demonstrated as proof-of-concepts within the Cadence Design & Functional Safety flow and the context of the ISO26262 using industrial case studies.

Recruitment host: Cadence Design Systems GmbH, Feldkirchen, DE
Cross-sectoral co-supervision (PhD studies): TU Delft, NL
Contact: Anton Klotz,
aklotz@cadence.com

ESR 4.3 Open-source EDA tools for design quality and reliability automation using zamiaCAD

ESR will study EDA methodologies and development of EDA tools for design quality and reliability in nanoelectronic systems. The project will exploit an open-source platform zamiaCAD with a front end for RTL descriptions and a scalable internal model. The platform has been already successfully applied for design error verification/debug and NBTI ageing modelling/mitigation. The ESR project will highly respect state-of-the-art industrial requirements and practices (e.g. scalability, formats and standards). As the result of the collaborative research performed in the RESCUE network, the new EDA tools will address approaches for functional validation, fault tolerance/resilience mechanisms and static and dynamic analysis of reliability threats (ageing, radiation-induced errors, etc.) at RTL as well as their automation.

Recruitment host: Computer Systems, Tallinn University of Technology, Tallinn, EE
Cross-sectoral co-supervision: IROC, FR
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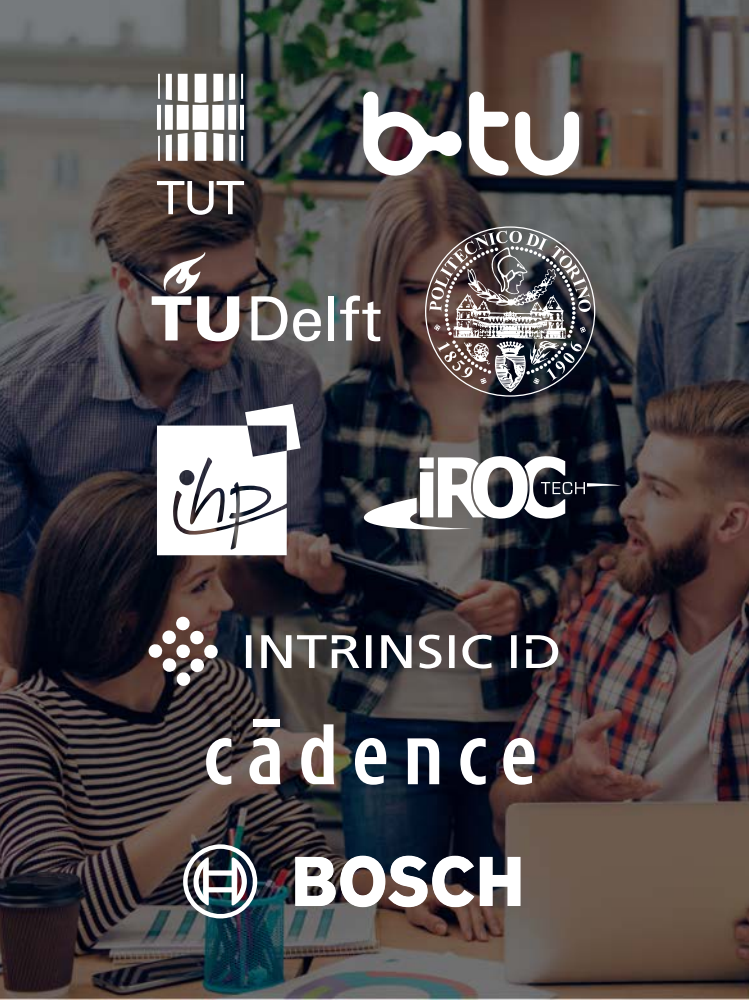

RESCUE Consortium

Beneficiaries / Partners:

Tallinn University of Technology, EE
BTU Cottbus-Senftenberg, DE
Delft University of Technology, NL
Politecnico di Torino, IT
Cadence Design Systems GmbH, DE
IROC Technologies, FR
Intrinsic-ID B.V., NL
IHP GmbH, DE

Partner Organisation:

Robert Bosch GmbH, DE

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